GF9330 High Performance HDTV/SDTV Deinterlacer

GF9330 Data Sheet

Features

- 10/8-bit progressive scan output up to 1080p60
- support for multiplexed and non-mutiplexed Y/C video
- multi-directional edge detection processing
- adaptive inter-field motion detection
- seamless interface to Gennum's GF9331 motion co-processor
- fully configurable to support custom video modes
- 3:2 film mode operation for HDTV/SDTV inputs
- programmable noise reduction and detail enhancement
- de-interlace, pass-through and film rate down conversion modes of operation
- seamless interface to popular ADCs and NTSC/PAL decoders
- ability to extract HVF information from embedded TRS
- selectable rounding and clipping of output data
- selectable blanking of active video lines
- HVF output signals with programmable output video cropping
- serial/parallel host interface
- 3.3V supply for device I/O and 2.5V for core logic
- 5V tolerant inputs

Applications

- HDTV Up/Down Converters
- Production Equipment
- Video Walls
- Projection Systems
- Plasma Displays
- LCD TVs
- Home Theatre Systems
- HD DVD Players

Device Overview

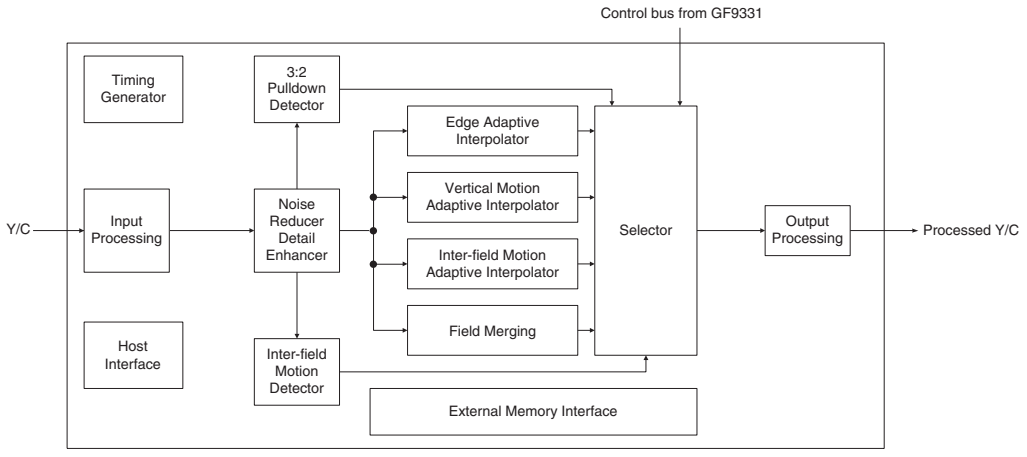
The GF9330 is a 10-bit high performance VDSP engine that performs high quality motion adaptive de-interlacing of interlaced digital video signals. The GF9330 supports standard definition (SDTV) and high definition (HDTV) signal formats and clock rates up to 1080p60 with support for arbitrary display modes.

The GF9330 uses multi-directional adaptive filters for edge processing, an adaptive vertical motion filter and an adaptive inter-field motion filter. The GF9330 features detail enhancement and noise reduction capabilities. The GF9330 also supports 3:2 pull-down, static/freeze-frame detection and compensation and film rate conversions. The GF9330 may operate as a stand-alone de-interlacer or may be used with the GF9331 Motion Co-processor to enable higher quality HD/SD de-interlacing with edge and vertical motion detection. The two devices can be configured in tandem such that the GF9331 sends edge detection and vertical motion filter control information to the GF9330. These control signals adaptively switch the GF9330's internal filters on a pixel-by-pixel basis.

The GF9330 integrates all required line delays and seamlessly interfaces to off chip SDRAMs that form the required field delays. The device may also operate in by-pass mode should no processing of the input signal be desired.

Ordering Information

Part Number	Package	Temp. Range
GF9330-CBP	328 PIN BGA	0^{o}C to 70^{o}C



Block Diagram

Contents

1. Pin Descriptions

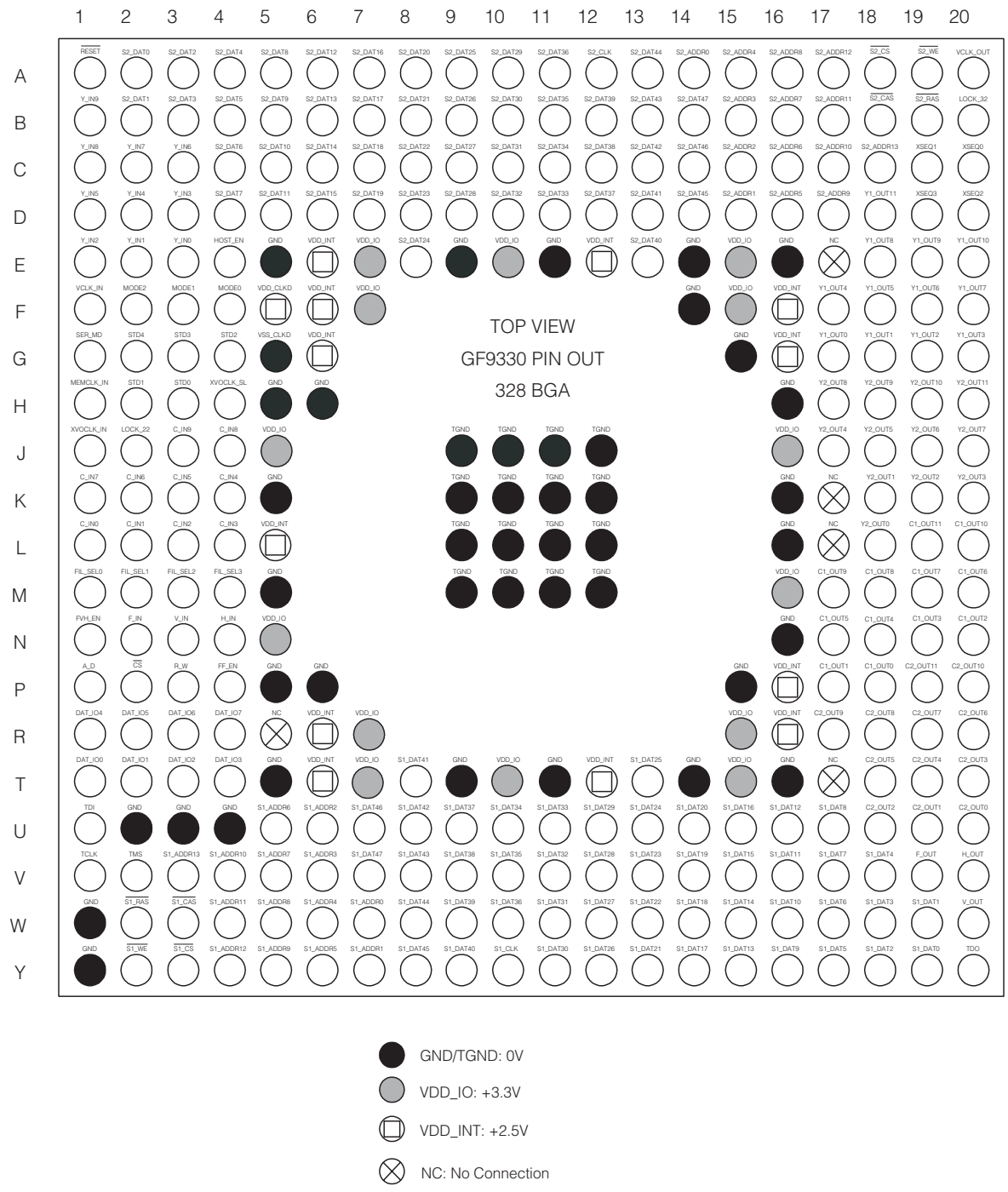


Figure 1-1: Top View Pin Out 328 BGA

Table 1-1: Pin Descriptions

Symbol	Pin Grid	Type	Description
$\overline{\text{RESET}}$	A1	I	Active low, asynchronous $\overline{\text{RESET}}$. Resets all internal logic to default conditions. Should be applied on power up.
VCLK_IN	F1	I	Video input clock. When the input is SDTV the input clock will be 27, 36, 54 or 72MHz. When the input format is HDTV, the input clock will be 74.25 or 74.25/1.001MHz.
MEMCLK_IN	H1	I	Memory clock for SDRAM operation to support HD modes, 90MHz input (supplied by an off-chip crystal oscillator).
XVOCLK_IN	J1	I	External video output clock. This input may be used instead of the internal VCLK_IN clock doubler to supply the video output clock VCLK_OUT.
XVOCLK_SL	H4	I	Control signal input. When HIGH, selects XVOCLK_IN; when LOW, selects the internal VCLK_IN clock doubler for generation of the video output VCLK_OUT signal.
Y_IN[9:0]	B1, C1, C2, C3, D1, D2, D3, E1, E2, E3	I	10/8-bit input bus for separate luminance or multiplexed luminance and colour difference video data. When supplying 8-bit data to the GF9330, Y_IN[1:0] will be set LOW and the 8-bit data supplied to Y_IN[9:2].
C_IN[9:0]	J3, J4, K1, K2, K3, K4, L4, L3, L2, L1	I	10/8-bit input bus for colour difference for video data. When supplying 8-bit data to the GF9330, C_IN[1:0] will be set LOW and the 8-bit data supplied to C_IN[9:2].
FIL_SEL[3:0]	M4, M3, M2, M1	I	Filter selection control bus. FIL_SEL[3:0] are used to switch the GF9330's internal directional filters on a pixel by pixel basis. FIL_SEL[3:0] is supplied by the GF9331.
F_IN	N2	I	Video timing control. F_IN identifies the ODD and EVEN fields in the incoming video signal. F_IN will be LOW in Field 1 and HIGH in Field 2.
V_IN	N3	I	Video timing control. V_IN represents the vertical blanking signal associated with the incoming video signal. V_IN is HIGH during the vertical blanking interval and LOW during active video.
H_IN	N4	I	Video timing control. H_IN represents the horizontal blanking signal associated with the incoming video signal. H_IN is HIGH during horizontal blanking and LOW during active video.
FVH_EN	N1	I	Control signal input. When HIGH, the F_IN, V_IN, and H_IN input pins will be used for video data signalling. When LOW, embedded TRS's will be detected for video data timing.
FF_EN	P4	I	Control signal input. When HIGH, FF_EN enables the GF9330's internal freeze frame compensation. See 3.11.4 Static and Freeze Frame Detection/ Compensation.
LOCK_22	J2	I	Control signal input. For 2:2 pull-down compensation, the LOCK_22 pin will be used to identify the presence of a 2:2 sequence in the input video stream.
STD[4:0]	G2, G3, G4, H2, H3	I	Video format definition. Defines the video standard when operating without the host interface. See Table 3-1: Encoding of STD[4:0] for Selecting Input Data Format.
MODE[2:0]	F2, F3, F4	I	Operating mode selection. Defines the mode of operation when operating without the host interface. See 3.9 Modes of Operation.

Table 1-1: Pin Descriptions (Continued)

Symbol	Pin Grid	Type	Description
HOST_EN	E4	I	Host interface enable. When set HIGH, the GF9330 will be configured through the host interface. On a high to low transition of HOST_EN the GF9330 will replace all register settings in the host interface with the values present on the external pins of the device including: STD[4:0], MODE[2:0], FVH_EN, FF_EN and XVOCLK_SL.
SER_MD	G1	I	Host interface mode selection. Enables serial mode operation when HIGH. Enables parallel mode operation when LOW.
$\overline{CS}$	P2	I	Functions as an active low chip select input for host interface parallel mode operation. Functions as a serial clock input for host interface serial mode operation.
DAT_IO[7:0]	R4, R3, R2, R1, T4, T3, T2, T1	I/O	Host interface bi-directional data bus for parallel mode. In serial mode, DAT[7] serves as the serial data output pin and DAT[0] serves as the serial data input pin.
R_W	P3	I	Host interface Read/Write control for parallel mode. A read cycle is defined when HIGH, a write cycle is defined when LOW.
A_D	P1	I	Host interface Address/Data control for parallel mode. The data bus contains an address when HIGH, a data word when LOW. In serial mode, this pin serves as the chip select (active low).
VCLK_OUT	A20	O	Video output clock. Output frequency based on selected output standard. See 3.9 Modes of Operation.
Y1_OUT[11:0]	D18, E20, E19, E18, F20, F19, F18, F17, G20, G19, G18, G17	O	Output data bus for separate luminance or multiplexed luminance and colour difference video data. See 3.10.2 12-bits Output Resolution.
Y2_OUT[11:0]	H20, H19, H18, H17, J20, J19, J18, J17, K20, K19, K18, L18	O	Output data bus for luminance video data during dual pixel mode operation. See 3.10.2 12-bits Output Resolution.
C1_OUT[11:0]	L19, L20, M17, M18, M19, M20, N17, N18, N19, N20, P17, P18	O	Output data bus for colour difference video data. See 3.10.2 12-bits Output Resolution.
C2_OUT[11:0]	P19, P20, R17, R18, R19, R20, T18, T19, T20, U18, U19, U20	O	Output data bus for colour difference video data during dual pixel mode operation. See 3.10.2 12-bits Output Resolution.
LOCK_32	B20	O	Control signal output. When the GF9330's internal algorithm detects a 3:2 sequence in the video stream the LOCK_32 signal is set HIGH. Otherwise, LOCK_32 is LOW.
XSEQ[3:0]	D19, D20, C19, C20	I/O	Control signal input/output. For external 3:2 sequence detection, the XSEQ[3:0] pins will be used to provide the 3:2 sequence information. For internal 3:2 detection the XSEQ[3:0] pins output the detected 3:2 sequence information. See Figure 3-12: Sequence Detection Input Signals.
H_OUT	V20	O	Output control signal. H_OUT is HIGH during horizontal blanking.
F_OUT	V19	O	Output control signal. F_OUT is LOW during field 1 and HIGH during field 2.
V_OUT	W20	O	Output control signal. V_OUT is HIGH during vertical blanking.
S1_CLK	Y10	O	SDRAM bank 1 clock.
$\overline{S1\_CS}$	Y3	O	Active low SDRAM chip select for Field Buffer 1.

Table 1-1: Pin Descriptions (Continued)

Symbol	Pin Grid	Type	Description
$\overline{\text{S1\_RAS}}$	W2	O	Active low SDRAM row address strobe for Field Buffer 1.
$\overline{\text{S1\_CAS}}$	W3	O	Active low SDRAM column address strobe for Field Buffer 1.
$\overline{\text{S1\_WE}}$	Y2	O	Active low SDRAM write enable for Field Buffer 1.
S1_ADDR[13:0]	V3, Y4, W4, V4, Y5, W5, V5, U5, Y6, W6, V6, U6, Y7, W7	O	SDRAM address for Field Buffer 1.
S1_DAT[47:0]	V7, U7, Y8, W8, V8, U8, T8, Y9, W9, V9, U9, W10, V10, U10, U11, V11, W11, Y11, U12, V12, W12, Y12, T13, U13, V13, W13, Y13, U14, V14, W14, Y14, U15, V15, W15, Y15, U16, V16, W16, Y16, U17, V17, W17, Y17, V18, W18, Y18, W19, Y19	I/O	SDRAM data for Field Buffer 1.
S2_CLK	A12	O	SDRAM bank 2 clock.
$\overline{\text{S2\_CS}}$	A18	O	Active low SDRAM chip select for Field Buffer 2.
$\overline{\text{S2\_RAS}}$	B19	O	Active low SDRAM row address strobe for Field Buffer 2.
$\overline{\text{S2\_CAS}}$	B18	O	Active low SDRAM column address strobe for Field Buffer 2.
$\overline{\text{S2\_WE}}$	A19	O	Active low SDRAM write enable for Field Buffer 2.
S2_ADDR[13:0]	C18, A17, B17, C17, D17, A16, B16, C16, D16, A15, B15, C15, D15, A14	O	SDRAM address for Field Buffer 2.
S2_DAT[47:0]	B14, C14, D14, A13, B13, C13, D13, E13, B12, C12, D12, A11, B11, C11, D11, D10, C10, B10, A10, D9, C9, B9, A9, E8, D8, C8, B8, A8, D7, C7, B7, A7, D6, C6, B6, A6, D5, C5, B5, A5, D4, C4, B4, A4, B3, A3, B2, A2	I/O	SDRAM data for Field Buffer 2.
TDI	U1	I	JTAG data input; connect to GND if not used.
TMS	V2	I	JTAG mode select; connect to GND if not used.
TCLK	V1	I	JTAG test clock; connect to GND if not used.
TDO	Y20	O	JTAG data output.
VDD_CLKD	F5	NA	2.5V supply for the internal clock doubler.
VSS_CLKD	G5	NA	Ground connection for the internal clock doubler.
VDD_IO	E7, E10, E15, F7, F15, J5, J16, M16, N5, R7, R15, T7, T10, T15	NA	3.3V supply.

Table 1-1: Pin Descriptions (Continued)

Symbol	Pin Grid	Type	Description
VDD_INT	E6, E12, F6, F16, G6, G16, L5, P16, R6, R16, T6, T12	NA	2.5V supply.
GND / TGND	E5, E9, E11, E14, E16, F14, G15, H5, H6, H16, K5, K16, L16, M5, N16, P5, P6, P15, T5, T9, T11, T14, T16, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, U2, U3, U4, W1, Y1	NA	Device ground / Thermal ground (electrically equivalent).
NC	E17, K17, L17, R5, T17		No connection.

2. Electrical Characteristics

2.1 5V Tolerant Inputs

Input cells used in the design are able to withstand 3.3V or 5V CMOS input signals without degrading performance or long-term reliability as well as TTL compatible inputs.

2.2 ESD Tolerance

GF9330 has 2kV ESD protection. ESD testing is done in accordance with Gennum's standard ESD testing procedure.

2.3 3.3V Supply for Device I/O and 2.5V for Core Logic

The GF9330 operates from a single +3.3V supply for device I/O, and a single +2.5V supply for core logic.

Table 2-1: Absolute Maximum Ratings

Parameter	Symbol	Value
Device I/O Supply Voltage	V_{DDIO}	-0.5 to TBD V
Device Core Supply Voltage	V_{DDCORE}	-0.5 to TBD V
Input Voltage Range (any input)	V_{IN}	$-0.5 < V_{IN} < +4.6V$
Operating Temperature Range	T_A	$0^oC < T_A < 70^oC$
Storage Temperature Range	T_S	$-40^oC < T_S < 125^oC$
Lead Temperature (soldering 10 seconds)		260^oC

Table 2-2: DC Electrical Characteristics

V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0 to 70°C, unless otherwise shown.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Device I/O Supply Voltage		V_{DDIO}	+3.0	+3.3	+3.6	V	a
Device Core Supply Voltage		V_{DDCORE}	+2.25	+2.5	+2.75	V	a
Device I/O Supply Current	V_{DDIO}=3.3V	I_{DDIO}	-	43	-	mA	a
Device Core Supply Current	V_{DDCORE}=2.5V	I_{DDCORE}	-	456	-	mA	a
Input Leakage Current	I_{IN}=0V or I_{IN}=V_{DD}	I_{LEAK}	-	-	10	µA	a

Table 2-2: DC Electrical Characteristics (Continued)

V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0 to 70°C, unless otherwise shown.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Tristate Leakage Current		$I_{TRILEAK}$	-	-	10	µA	a
Input Logic LOW Voltage		V_{IL}	-	-	0.8	V	a
Input Logic HIGH Voltage		V_{IH}	2.1	-	-	V	a
Output Logic LOW Voltage	I_{OL}= 4mA	V_{OL}	-	0.2	0.4	V	a
Output Logic HIGH Voltage	I_{OH}= -4mA	V_{OH}	2.7	-	-	V	a

a. Production, test and QA are performed at room temperature.

Table 2-3: AC Electrical Characteristics - Video Interfaces

The Video Interface signals include: VCLK, Y_IN[9:0}, C_IN[9:0}, FIL_SEL[3:0], F_IN, V_IN, H_IN, FVH_EN, FF_EN, LOCK_22, Y1_OUT[11:0], Y2_OUT[11:0], C1_OUT[11:0], C2_OUT[11:0], LOCK_32, XSEQ[3:0], H_OUT, F_OUT and V_OUT.

V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0 to 70°C, unless otherwise shown.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Clock Input Frequency		F_{HSCI}	-	74.25	83	MHz	a, b
Input Data Setup Time		t_{SU}	2.5	-	-	ns	a, c
Input Data Hold Time		t_{IH}	1.5	-	-	ns	a, c
Input Clock Duty Cycle			40	-	60	%	a
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD}	-	-	10.0	ns	a
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH}	2.0	-	-	ns	a
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN}	-	-	10	ns	a
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS}	-	-	10	ns	a
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF}	-	-	2.0	ns	a, d

a.Based on simulation results, verified during device characterization process.
b.Also supports 74.25/1.001MHz.
c.50% levels.
d.20% to 80% levels.

Table 2-4: AC Electrical Characteristics - SDRAM Interfaces

The SDRAM 1 Interface signals include S1_CLK, $\overline{\text{S1\_CS}}$, $\overline{\text{S1\_RAS}}$, $\overline{\text{S1\_CAS}}$, $\overline{\text{S1\_WE}}$, S1_ADDR[13:0] and S1_DAT[47:0].
The SDRAM 2 Interface signals include S2_CLK, $\overline{\text{S2\_CS}}$, $\overline{\text{S2\_RAS}}$, $\overline{\text{S2\_CAS}}$, $\overline{\text{S2\_WE}}$, S2_ADDR[13:0] and S2_DAT[47:0].
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0 to 70ºC, unless otherwise shown.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Clock Input Frequency		F_{HSCI_SD}	-	85	90	MHz	a
Input Data Setup Time		t_{SU_SD}	2.0	-	-	ns	a, b
Input Data Hold Time		t_{IH_SD}	2.5	-	-	ns	a, b
Input Clock Duty Cycle			40	-	60	%	a
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD_SD}	-	-	9.1	ns	a
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH_SD}	2.0	-	-	ns	a
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN_SD}	-	-	20	ns	a, c
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS_SD}	-	-	20	ns	a, c
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF_SD}	-	-	2.0	ns	a, d

a.Based on simulation results, verified during device characterization process.
b.50% levels.
c.Two clock cycles allocated for data bus turnaround.
d.20% to 80% levels.

Table 2-5: AC Electrical Characteristics - Host Interfaces

The Host Interface signals include HOST_EN, SER_MD, $\overline{\text{CS}}$, DAT_IO[7:0], R_W and A_D.
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0 to 70ºC, unless otherwise shown.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Clock Input Frequency		F_{HSCI_HI}	-	-	20	MHz	a
Input Data Setup Time		t_{SU_HI}	5	-	-	ns	a, b
Input Data Hold Time		t_{IH_HI}	1.5	-	-	ns	a, b
Input Clock Duty Cycle			40	-	60	%	a
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD_HI}	-	-	10.0	ns	a

Table 2-5: AC Electrical Characteristics - Host Interfaces (Continued)

The Host Interface signals include HOST_EN, SER_MD, $\overline{CS}$, DAT_IO[7:0], R_W and A_D.
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0 to 70°C, unless otherwise shown.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH_HI}	2.0	-	-	ns	a
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN_HI}	-	-	15	ns	a
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS_HI}	-	-	15	ns	a
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF_HI}	-	-	2.0	ns	a, c

a.Based on simulation results, verified during device characterization process.
b.50% levels.
c.20% to 80% levels.

3. Detailed Device Description

3.1 Supported Input Video Formats

The GF9330 supports multiple input data formats with multiplexed or separate Y/C channels. Data is supplied to the GF9330 through the Y_IN[9:0] and the C_IN[9:0] busses. Table 3-1: Encoding of STD[4:0] for Selecting Input Data Format outlines the data formats that are supported according to the setting of the control register bits STD[4:0]

NOTE: For all progressive video standards the GF9330 must be manually set to bypass mode (MODE[2:0] = 111). See 3.5 Host Interface for details.

Table 3-1: Encoding of STD[4:0] for Selecting Input Data Format

STD	STD[4:0]	Description
0	00000	525i (30/1.001) component SMPTE 125M. Multiplexed YCbCr data applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 27MHz.
1	00001	Reserved
2	00010	525i (30/1.001) component 16x9 SMPTE 267M. Multiplexed YCbCr data applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 36MHz.
3	00011	Reserved
4	00100	625i (25Hz) component EBU tech. 3267E. Multiplexed YCbCr data applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 27MHz.
5	00101	Reserved
6	00110	625i (25Hz) component 16x9 ITU-R BT.601-5 Part B. Multiplexed YCbCr data applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 36MHz.
7	00111	Reserved
8	01000	525p (60/1.001Hz) SMPTE 293M. YCbCr data stream applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 54MHz.
9	01001	Reserved
10	01010	Reserved
11	01011	Reserved
12	01100	625p (50Hz) ITU-R BT.1358. YCbCr data stream applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 54MHz.
13	01101	625p (50Hz) 16 x 9 with 18MHz sampling. YCbCr data stream applied to Y_IN. C_IN is set LOW. NOTE: Input clock is 72MHz.
14	01110	Generic SD input data format with 4:1:1 sampling. YCbCr data is applied to both Y_IN and C_IN. Externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. NOTE: Input clock is 27MHz.

Table 3-1: Encoding of STD[4:0] for Selecting Input Data Format (Continued)

STD	STD[4:0]	Description
15	01111	Generic SD input data format with 4:2:2 sampling and single multiplexed YCbCr input format. YCbCr data applied to Y_IN. C_IN is set LOW. Externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. NOTE: Input clock is 27 or 36MHz.
16	10000	720p (60 & 60/1.001Hz) SMPTE 296M-2001. Y Data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25 MHz or 74.25/1.001MHz.
17	10001	720p (30 & 30/1.001Hz) SMPTE 296M-2001. Y Data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.2 or 74.2/1.001MHz.
18	10010	1080p (30 & 30/1.001Hz) SMPTE 274M. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.
19	10011	720p (50Hz) SMPTE 296M-2001. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
20	10100	1080p (25Hz) SMPTE 274M. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
21	10101	720p (25Hz) SMPTE 296M-2001. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
22	10110	1080p (24 & 24/1.001Hz) SMPTE 274M. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.
23	10111	720p (24 & 24/1.001Hz) SMPTE 296M-2001. Y Data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.
24	11000	1080i (30 & 30/1.001Hz) SMPTE 274M. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.
25	11001	1080p (30 & 30/1.001Hz in Segmented Frame Format) SMPTE RP211-2000. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.
26	11010	1080i (25Hz) SMPTE 274. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
27	11011	1080p (25 Hz in Segmented Frame Format) SMPTE RP211-2000. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
28	11100	1080i (25Hz) SMPTE 295M. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
29	11101	1080p (24 & 24/1.001Hz in Segmented Frame Format) SMPTE RP211-2000. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.

Table 3-1: Encoding of STD[4:0] for Selecting Input Data Format (Continued)

STD	STD[4:0]	Description
30	11110	1035i (30Hz) SMPTE 260M. Y data applied to Y_IN. Cb Cr data applied to C_IN. NOTE: Input clock is 74.25MHz.
31	11111	Generic HD input data format with 4:2:2 sampling and a separate Y/C format. Y data applied to Y_IN. Cb Cr data applied to C_IN. Externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. NOTE: Input clock is 74.25MHz or 74.25/1.001MHz.

3.2 Input Synchronization

The GF9330 obtains relevant timing information from either embedded TRS information or externally supplied H_IN, V_IN and F_IN signals.

When FVH_EN is set HIGH, using either the host interface or the external pin, the GF9330 relies on the externally supplied H_IN, V_IN and F_IN signals for timing information. When FVH_EN is set LOW, the GF9330 will extract the embedded TRS timing information from the video data stream and will ignore any timing information present on the F_IN, V_IN and H_IN pins.

3.2.1 Support for Both 8-bit and 10-bit Input Data

The GF9330 supports 8 and 10-bit input data. When operating with 8-bit input data, the two LSBs of the GF9330's 10-bit input should be set LOW and the input data is applied to the 8 MSBs of the input bus.

3.2.2 Generic Input Format Signalling

The GF9330 supports generic input data formats with either 4:1:1 or 4:2:2 sampling structures handling up to 2046 active samples per line with a total maximum line width of 4096 (active + blanking) samples. In addition, there is a limit of 2048 lines per interlaced frame. The following host interface parameters are used to describe the generic input data format relative to the F_IN, V_IN and H_IN signals. See Figure 3-1: Generic Input Format Definition.

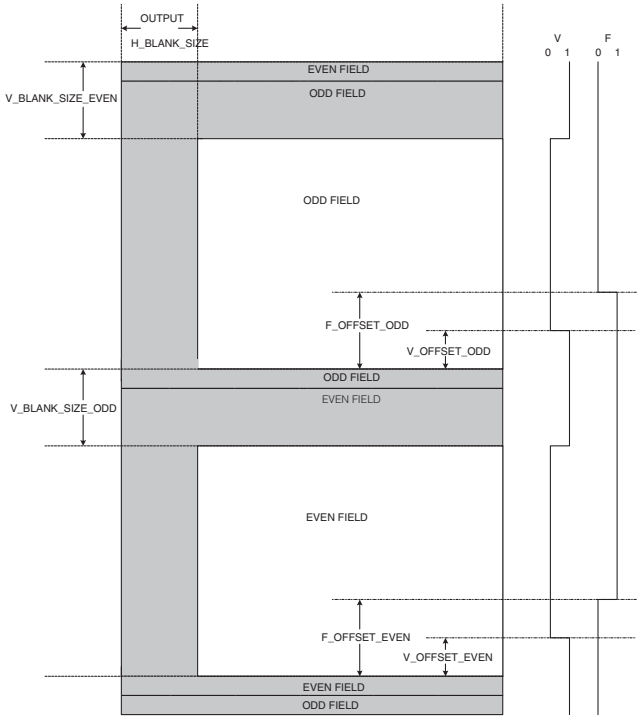


Figure 3-1: Generic Input Format Definition

3.2.2.1 OUTPUT H_BLANK_SIZE

This parameter defines the number of samples that comprise the horizontal blanking region. This parameter has a maximum value of 4095 and is to be less than the total line width (active + blanking) sample size. Twelve bits within the host interface are dedicated to this parameter. The GF9330 only stores and processes active video samples only (i.e. H_IN=0).

3.2.2.2 V_BLANK_SIZE_ODD

This parameter defines the number of lines that comprise the vertical blanking interval that follows the odd field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. The GF9330 only stores and processes active video samples (i.e. V_IN=0). See Figure 3-1: Generic Input Format Definition.

3.2.2.3 V_BLANK_SIZE_EVEN

This parameter defines the number of lines that comprise the vertical blanking interval that follows the even field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. The GF9330 only stores and processes active video samples (i.e. V_IN=0). See Figure 3-1: Generic Input Format Definition.

3.2.2.4 V_OFFSET_ODD

This defines the number of lines from the V_IN pin EAV transition to the end of the odd active video field region. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which that output non-standard timing for the V_IN signal. See Figure 3-2: Vertical Offset Definition.

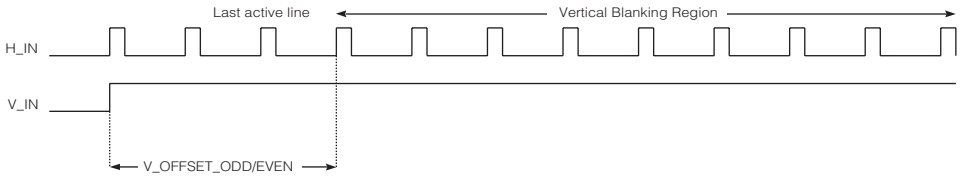


Figure 3-2: Vertical Offset Definition

3.2.2.5 V_OFFSET_EVEN

This parameter defines the number of lines from the V_IN pin EAV transition to the end of the even active video field region. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders that output non-standard timing for the V_IN signal. See Figure 3-2: Vertical Offset Definition.

3.2.2.6 F_OFFSET_ODD

This defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the odd field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders that output non-standard timing for the F_IN signal. See Figure 3-1: Generic Input Format Definition.

3.2.2.7 F_OFFSET_EVEN

This register defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the even field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the F_IN signal. See Figure 3-1: Generic Input Format Definition.

3.2.2.8 H_POLARITY

This register defines the polarity of the H_IN pin. With H_POLARITY set LOW, a falling transition on the H_IN pin indicates end of active video. With H_POLARITY set HIGH, a rising transition on the H_IN pin indicates the end of active video. One bit within the host interface is dedicated to this parameter.

3.2.2.9 F_POLARITY

This register defines the polarity of the F_IN pin. Refer to Table 3-2: F_POLARITY for F_POLARITY encoding. One bit within the host interface is dedicated to this parameter.

Table 3-2: F_POLARITY

F_POLARITY Register	F_IN Pin	F_IN Pin Function
0	0	Even Field
0	1	Odd Field
1	0	Odd Field
1	1	Even Field

3.2.2.10 V_POLARITY

This register defines the polarity of the V_IN pin. With V_POLARITY set LOW, a falling transition on the V_IN pin indicates the end of active video. With V_POLARITY set HIGH, a rising transition on the V_IN pin indicates the end of active video. One bit within the host interface is dedicated to this parameter.

3.3 Seamless Interface to the GF9331 Motion Co-processor for Directional Filter Control

The GF9330 can operate as a stand-alone motion adaptive de-interlacer or can operate in conjunction with the GF9331 Motion Co-processor. The GF9331 contains adaptive multi-directional edge detection and vertical motion detection. Control signals are fed back directly to the GF9330.

These control signals adaptively switch the GF9330's internal edge & vertical motion de-interlacing filters on a pixel by pixel basis. These control signals are fed to the GF9330 by the GF9331 over the FIL_SEL[3:0] control bus. When the GF9330 is not being used with the GF9331, the FIL_SEL[3:0] inputs should be set LOW.

NOTE*:* When using the GF9331, the Y_IN[9:0] of the GF9330 must be connected to Y_OUT[9:0] of the GF9331 and C_IN[9:0] of the GF9330 must be connected to the C_OUT[9:0] of the GF9331. FIL_SEL[3:0] of the GF9330 must also be connected to FIL_SEL[3:0] of the GF9331. The timing information from the GF9331 is provided exclusively through the F_OUT, H_OUT and V_OUT pins which must be connected to the F_IN, H_IN and V_IN pins of the GF9330.

3.4 Seamless Interface to External SDRAMs

For all SD video formats, the GF9330 requires two 1M x 24-bit (min.) SDRAM field buffers.

To pass HD video formats in bypass mode, the GF9330 requires two field buffers, each implemented with a 1M x 48-bit (min.) SDRAM configuration. To deinterlace HD formats, the memory requirements increase to a 4M x 48-bit (min) SDRAM configuration.

Table 3-3: SDRAM Configuration

Format	Bypass	Configuration per Bank[a]	Total of ADDR and BANK[b]	SDRAM properties (per bank)			Recomended
				Min. Freq. (MHz)	Min. Access Time (ns)	CAS Latency	
SD	Yes	1(1Mx24)	12	90	5.5	3	Micron: MT48LC4M16A2, MT48LC8M16A2
	No	1(1Mx24	12	90	5.5	3	
HD	Yes	1(1Mx48)	12	90	5.5	3	
	No	1(1Mx48)	14	90	5.5	3	

a.There are 2.
b.This is assuming a 8-column structure.

3.5 Host Interface

The GF9330 provides both a serial and parallel host interface control port for the configuration of internal parameters. The GF9330 is also able to operate in stand-alone mode, with no host interface control. In stand-alone mode, the video standard (STD[4:0]) and mode of operation (MODE[2:0]) are set using dedicated pins on the device. These values are loaded into the device on a falling transition of HOST_EN or after setting $\overline{\text{RESET}}$ LOW.

Both the serial and parallel interfaces share common pins as described in Table 3-4: Host Interface Common Pins.

Table 3-4: Host Interface Common Pins

GF9330 PIN NAME	PARALLEL MODE	SERIAL MODE
$\overline{\text{CS}}$	CHIP select	SCLK - Serial Clock
DAT_IO[0]	Data/address (bit 0)	SDI - Serial data in
DAT_IO[1]	Data/address (bit 1)	(not used)
DAT_IO[2]	Data/address (bit 2)	(not used)
DAT_IO[3]	Data/address (bit 3)	(not used)
DAT_IO[4]	Data/address (bit 4)	(not used)

Table 3-4: Host Interface Common Pins (Continued)

GF9330 PIN NAME	PARALLEL MODE	SERIAL MODE
DAT_IO[5]	Data/address (bit 5)	(not used)
DAT_IO[6]	Data/address (bit 6)	(not used)
DAT_IO[7]	Data/address (bit 7)	SDO - Serial data out
A_D	Address/data select	$\overline{SCS}$ - Serial chip select
R_W	Read/write select	(not used)
HOST_EN	Host Interface enable	Host Interface enable
SER_MD	LOW = Parallel mode enable	HIGH = Serial mode enable

3.5.1 Host Interface Serial Mode

The Gennum Serial Peripheral Interface (GSPI) is a 4 wire interface comprised of serial data in (SDI), serial data out (SDO), an active LOW serial chip select ($\overline{SCS}$) and a clock (SCLK). The interface operates in a master/slave configuration, where the master provides the SCLK, SDI, and $\overline{SCS}$ signals to the slave or slaves. The master uC_SDO drives the slave(s) SDI input. The SDO pin is a tristate output that allows multiple devices to drive the master uC_SDI. Serial mode operation supports both a continuous clock and a burst clock configuration. The serial mode interface is illustrated in the Figure 3-3: Host Interface Serial Mode.

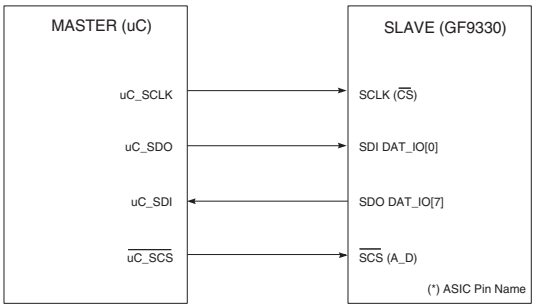


Figure 3-3: Host Interface Serial Mode

3.5.1.1 Serial Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Configure control bit, nine reserved bits and a 5-bit address. As shown in Figure 3-4: Serial Command Word Bit Representation.

Figure 3-4: Serial Command Word Bit Representation

The R/W bit indicates a Read command if R/W = HIGH, and a write command when R/W = LOW.

3.5.1.2 Auto-Configure

The Auto-Configure feature will be executed when the Auto-Configure control bit is set. All Auto-Configure registers will be updated to their appropriate settings based on the current video standard and operational mode.

When setting the Auto-Configure bit, the command word should be set with only the AC bit set to 1. All of the 15 remaining bits should be set to 0. To complete the Auto-Configuration 16 additional bits must be loaded into the device. The state of these bits can be either HIGH or LOW. Before Auto-Configuring the device, the standard and mode must be set using either the host interface (HOST_EN = 1) or the external pins (with a falling transition of HOST_EN).

This simplifies configuration while allowing customization of many features and format parameters.

3.5.1.3 Serial Data Word Description

The serial data word consists of a 16-bit word as shown in Figure 3-5: Serial Data Word Bit Representation. Serial data is transmitted or received MSB first.

Figure 3-5: Serial Data Word Bit Representation

Both command and data words are clocked into the GF9330 on the rising edge of the serial clock (SCLK), which may operate in either a continuous or burst fashion. The first bit (MSB) of the serial output (SDO) is available following the last falling SCLK edge of the "read" command word. The remaining bits are clocked out on the falling edges of SCLK.

3.5.1.4 Serial Write Operation

All write cycles consist of a command word followed by a data word, both transmitted to the GF9330 via SDI. The first 16-bit word transmitted following a falling transition of $\overline{SCS}$ is a command word. Several write cycles may be performed while $\overline{SCS}$ is LOW. See Figure 3-6: Write Cycle.

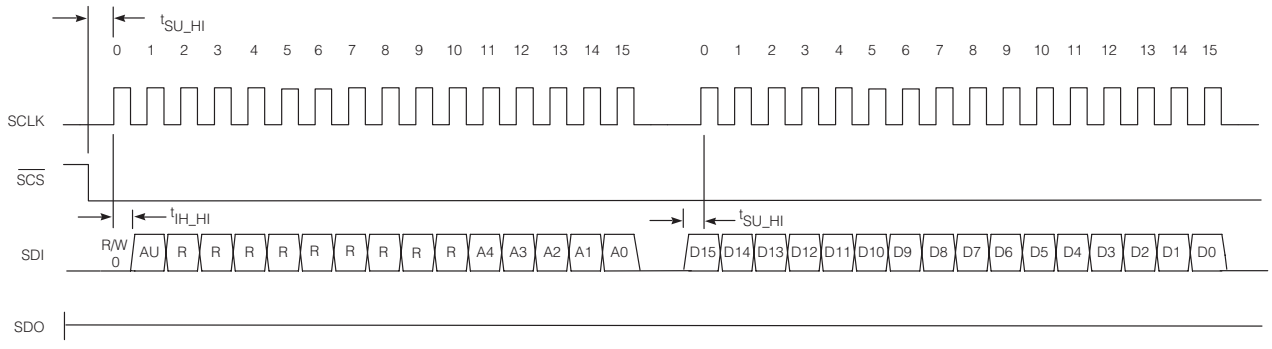


Figure 3-6: Write Cycle

3.5.1.5 Serial Read Operation

All read cycles consist of a command word transmitted to the GF9330 via SDI followed by a data word transmitted from the GF9330 via SDO. The first 16-bit word transmitted following a falling transition of $\overline{SCS}$ is a command word. Several read cycles may be performed while $\overline{SCS}$ is LOW. See Figure 3-7: Read Cycle.

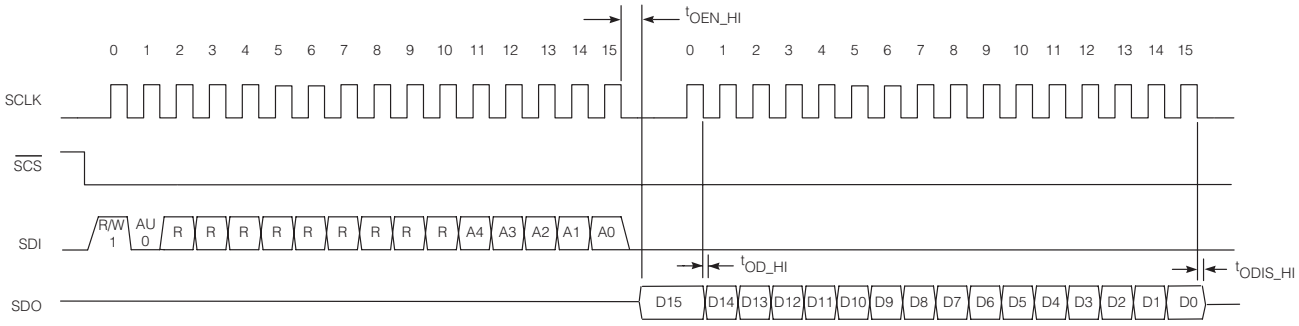


Figure 3-7: Read Cycle

3.5.2 Host Interface Parallel Mode

The Gennum Parallel Peripheral Interface (GPPI) consists of an 8-bit multiplexed address/data bus (DAT_IO[7:0]), a chip select pin ($\overline{CS}$), a read/write pin (R_W), and an address/data pin (A_D) as shown in Figure 3-8: Parallel Peripheral Interface.

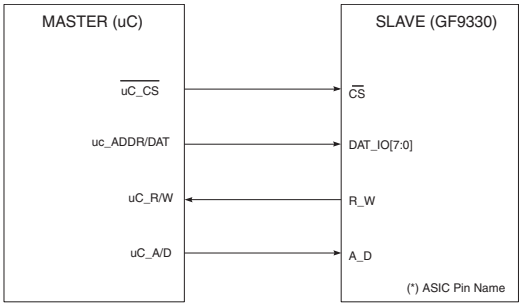


Figure 3-8: Parallel Peripheral Interface

Data is strobed in/out of the parallel interface on the falling edge of $\overline{CS}$. The GF9330 drives the DAT_IO[7:0] bus when the R_W pin is HIGH and the $\overline{CS}$ pin is LOW, otherwise this port is in a high impedance state.

3.5.2.1 Parallel Address Word Description

The 8-bit address word loads in the address to be accessed and allows the Auto-Configure bit to be set. The MSB is the Auto-Configure bit, followed by two reserved bits and a 5-bit address as shown in Figure 3-9: Parallel Address Word Bit Representation.

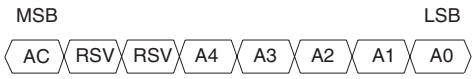


Figure 3-9: Parallel Address Word Bit Representation

3.5.2.2 Parallel Write Operation

A write cycle to the parallel interface is shown in Figure 3-10: Write Cycle to the Parallel Interface. First an 8-bit address word is provided to the DAT_IO bus by asserting the R_W pin to LOW and the A_D pin to HIGH. The MSB of the address word contains an auto-update flag, which allows automatic configuration of predefined registers. The 5 LSB's of the address word contain the address location for the read or write operation. The remaining address bits DAT_IO[6:5] are reserved. The address word is registered on the falling edge of $\overline{CS}$. Following this, the A_D pin is driven LOW and two data words are sent upper byte (UB) word first and are each clocked in on the falling edge of $\overline{CS}$. Two 8-bit data words must follow each address word to occupy each 16-bit parameter, which are defined in Figure 3-11: Host Interface Register Allocation.

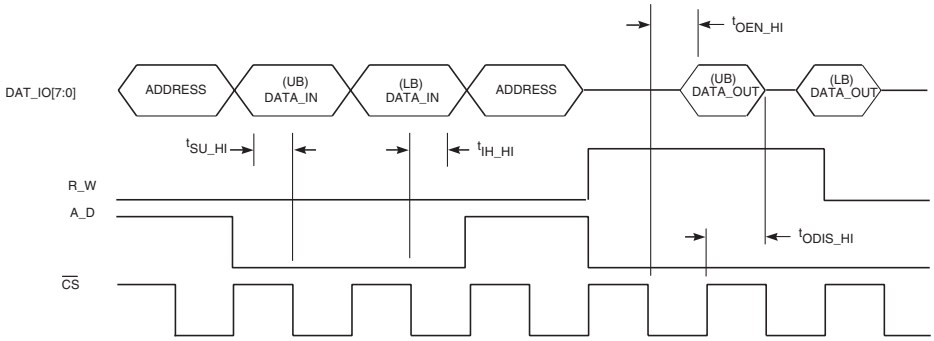


Figure 3-10: Write Cycle to the Parallel Interface

3.5.2.3 Parallel Read Operation

A read cycle begins with an address write by asserting the R_W pin LOW and the A_D pin HIGH. The address is clocked on the falling edge of $\overline{CS}$. Following the address, the R_W pin must be driven HIGH and A_D pin driven LOW to allow the upper byte of data to be clocked out on the first falling edge of $\overline{CS}$ followed by the lower byte on the second falling edge of $\overline{CS}$.

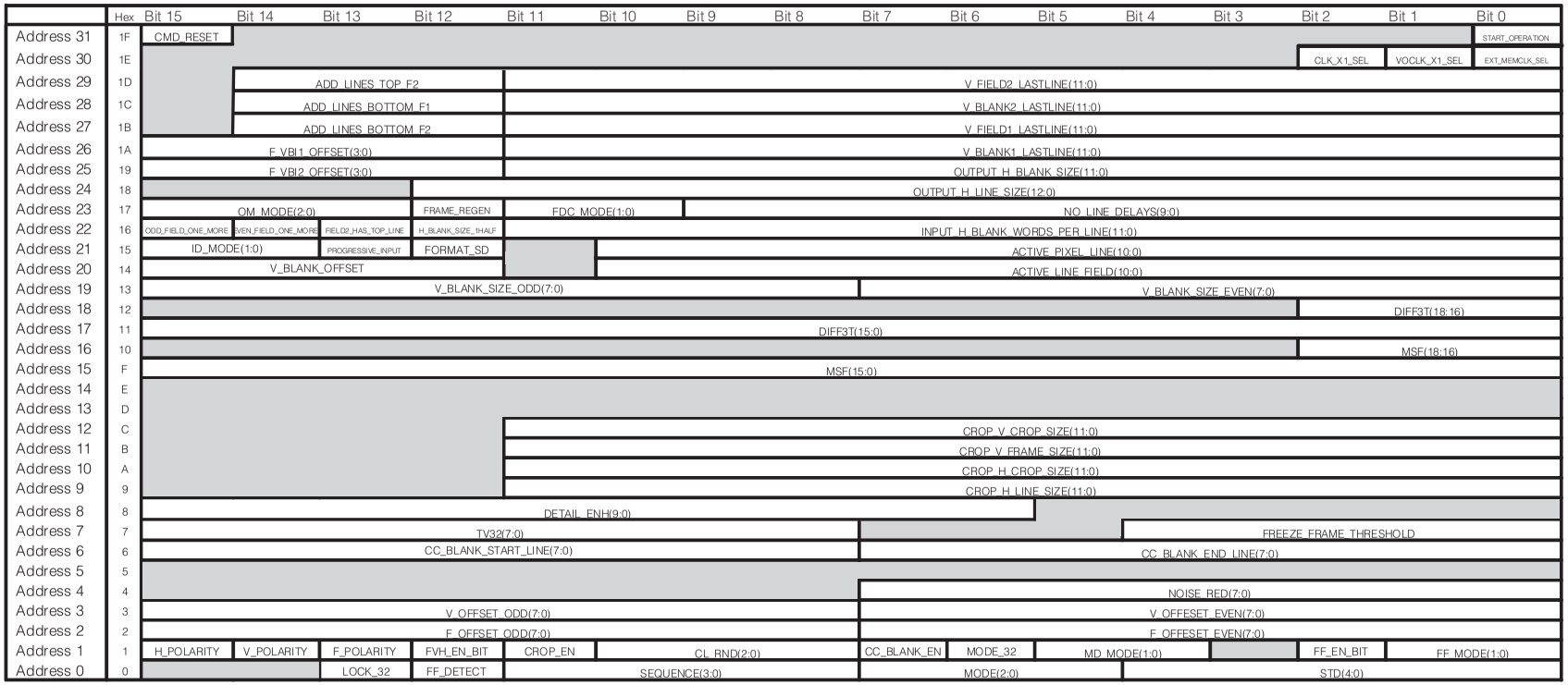


Figure 3-11: Host Interface Register Allocation

3.5.3 Control Register Definitions

The host interface internal registers are divided into three classes: User Configurable (UC), Auto-Configurable (AC), and Read-Only (RO). Address locations 0 through 14 contain parameters which may be configured by the user. Locations 15 through 31 are automatically configured based on the STD[4:0] and MODE[2:0] registers, but can be user configured if desired.

Address 0 contains three status registers LOCK_32, FF_DETECT, and SEQUENCE[3:0] which can only be read. Writing to the read-only registers will have no effect on their contents.

Table 3-5: Control Register Definitions

Address	Bit Location	Register Name	Class	Description	Default
0	4:0	STD[4:0]	UC	Defines the video standard as described in 3.1 Supported Input Video Formats.	00000
	7:5	MODE[2:0]	UC	Defines the GF9330 operating mode: 000: Interlaced to Progressive Mode 001: Field Merging Mode 010: Film Rate Down Conversion Mode 011: Film Rate Down Conversion (Progressive Segmented Frame) Mode 111: Bypass Mode (Video Pass Through Mode)	000
	11:8	SEQUENCE[3:0]	RO	Provides the detected field sequence number from the 3:2 detection circuit.	Calculated
	12	FF_DETECT	RO	Set to '1' if a video freeze frame has been detected.	Calculated
	13	LOCK_32	RO	Set to '1' if a 3:2 video sequence has been detected.	Calculated

Table 3-5: Control Register Definitions (Continued)

Address	Bit Location	Register Name	Class	Description	Default
1	1:0	FF_MODE[1:0]	UC	Defines the freeze frame operating mode: 00: Manual freeze frame detection/compensation 01: Automatic freeze frame detection/compensation (default value) 10: Disabled 11: Reserved	01
	2	FF_EN_BIT	UC	Enables (1) or disables (0) freeze frame detection / compensation when in manual freeze frame mode, i.e. FF_MODE = 00.	01
	5:4	MD_MODE[1:0]	UC	Defines the motion detection and compensation mode: 00: Disabled 01: Automatic 10: Reserved 11: Reserved	01
	6	MODE_32	UC	Selects the internal 3:2 sequence detection when set to 0, otherwise uses external sequence from the input pins, XSEQ[3:0].	0
	7	CC_BLANK_EN	UC	Enables blanking in the close captioned video region.	0
	10:8	CL_RND[2:0]	UC	Defines the clipping and rounding output format: 000: 12-bit output with 10.2 (.25 lsb) resolution 001: 10-bit output clipped/rounded from 0 to 1023 010: 10-bit output clipped/rounded from 4-1019 011: 10-bit output Y clipped/rounded from 64 to 940, Cr/Cb clipped/rounded from 64 to 960 100: Reserved 101: 8-bit output clipped/rounded from 0 to 255 110: 8-bit output rounded/clipped from 1 to 254 111: 8-bit output Y clipped/rounded from 16 to 235, Cr/Cb clipped/rounded from 16 to 240	000
	11	CROP_EN	UC	Enables output video cropping based on CROP_V_CROP_SIZE, CROP_V_FRAME_SIZE, CROP_H_CROP_SIZE and CROP_H_LINE_SIZE parameters.	0
	12	FVH_EN_BIT	UC	Enables the GF9330 to use external FVH control in place of embedded TRS.	0
	13	F_POLARITY	UC	Defines the polarity of the F_IN pin. When set to '1', F follows normal convention where F_IN is '0' for field 1(odd) and '1' for field 2 (even).	1
	14	V_POLARITY	UC	Defines the polarity of the V_IN pin. When set to '1', V_IN follows normal convention where V_IN is '1' in the vertical blanking region.	1
	15	H_POLARITY	UC	Defines the polarity of the H_IN pin. When set to '1', H_IN follows normal convention where H is '1' in the horizontal blanking region.	1

Table 3-5: Control Register Definitions (Continued)

Address	Bit Location	Register Name	Class	Description	Default
2	7:0	F_OFFSET_EVEN[7:0]	UC	Defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the even field. This parameter has a maximum value of 255.	00000000
	15:8	F_OFFSET_ODD[7:0]	UC	Defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the odd field. This parameter has a maximum value of 255.	00000000
3	7:0	V_OFFSET_EVEN[7:0]	UC	Defines the number of lines from the V_IN pin EAV transition to the end of the even active video field region. This parameter has a maximum value of 255.	00000000
	15:8	V_OFFSET_ODD[7:0]	UC	Defines the number of lines from the V_IN pin EAV transition to the end of the odd active video field region. This parameter has a maximum value of 255.	00000000
4	7:0	NOISE_RED[7:0]	UC	The upper five bits of this parameter adjust the noise reduction level applied to the video image, the resolution of the adjustment is defined by the lower 3-bits: Noise Reduction = Y / X Y = NOISE_RED[7:3] X = NOISE_RED[2:0] 0 <= Y <= 31 X = 1 | 2 | 4 A higher value represents more noise reduction with greater resolution.	00100001
	15:8	STANDARD CONFIGURATION REGISTERS	UC	Must be set to default value.	01000100
5	15:0	FF_DET_HV[15:0]	UC	Freeze frame detection setting. See 3.11.4 Static and Freeze Frame Detection/Compensation	IE32H
6	7:0	CC_BLANK_END_ LINE[7:0]	UC	Defines the last line number at which to end closed captioned blanking. For this parameter, line 0 is defined as the first active line of the field/frame.	0000000
	15:8	CC_BLANK_START_ LINE[7:0]	UC	Defines the first line number at which to start closed captioned blanking. For this parameter, line 0 is defined as the first active line of the field/frame.	00000000
7	4:0	FREEZE_FRAME_ THRESHOLD[4:0]	UC	Defines the freeze frame detection threshold, a low value causes noise to have a larger impact on freeze frame detection.	10000 (16 decimal)
	15:9	TV32[7:0]	UC	Defines the threshold for the detection of vertical motion between two consecutive fields. A higher value will increase the sensitivity.	00101000 (40 decimal)

Table 3-5: Control Register Definitions (Continued)

Address	Bit Location	Register Name	Class	Description	Default
8	5:0	STANDARD CONFIGURATION REGISTERS	UC	Must be set to default value.	100100
	15:6	DETAIL_ENH[9:0]	UC	Defines the detail enhancement configuration. The upper five bits of this word adjust the high frequency detail in the image. The lower 5-bits control the resolution or granularity. A higher value represents more detail with higher granularity. Detail Enhancement = Y / X Y = DETAIL_ENH[9:5] X = DETAIL_ENH[4:0] 0 <= Y <= 31 X = 1 | 2 | 4 | 8 | 16	0000000001
9	11:0	CROP_H_LINE_SIZE [11:0]	UC	Specifies the length of the line to output, following the cropped pixels on the left side of the line.	000000000000
10	11:0	CROP_H_CROP_SIZE [11:0]	UC	Specifies the number of active pixels to blank at the beginning of each line.	000000000000
11	11:0	CROP_V_FRAME_ SIZE[11:0]	UC	Specifies the number of lines to output, following the cropped lines at the top of the frame (or field).	000000000000
12	11:0	CROP_V_CROP_ SIZE[11:0]	UC	Specifies the number of active lines to blank at the beginning of each frame.	000000000000
14,13	2:0, 15:0	STANDARD CONFIGURATION REGISTERS	UC	Must be set to default value.	00080H (128 decimal)
16,15	2:0, 15:0	MSF[18:0]	UC	Represents the number of pixels per smallest active field divided by a scaling factor required to estimate same frame detection. A higher value also means vertical edges will have more effect on the detection of same frames. The equation is as follows: MSF = #active_pixels_per_smallest_field / 2^7	Calculated
18, 17	2:0, 15:0	DIFF3T[18:0]	UC	Represents the number of active pixels per smallest field divided by a factor required to estimate the odd and even pattern detection. The equation is as follows: DIFF3T = #active_pixels_per_smallest_field /2^7	Calculated
19	7:0	V_BLANK_SIZE_ EVEN[7:0]	AC	Defines the number of lines that comprise the vertical blanking interval that follows the even input field. This parameter has a maximum value of 255.	Auto
	15:8	V_BLANK_SIZE_ ODD[7:0]	AC	Defines the number of lines that comprise the vertical blanking interval that follows the odd input field. This parameter has a maximum value of 255.	Auto
20	10:0	ACTIVE_LINE_ FIELD[10:0]	AC	Defines the number of active lines per smallest input field.	Auto
	15:12	V_BLANK_OFFSET [3:0]	AC	For 3:2 pull-down compensation, this parameter must provide the difference (if any) in number of input active lines per frame and the number of output active lines per frame.	Auto

Table 3-5: Control Register Definitions (Continued)

Address	Bit Location	Register Name	Class	Description	Default
21	10:0	ACTIVE_PIXEL_ LINE[10:0]	AC	Defines the number of active pixels per video input line.	Auto
	12	FORMAT_SD	AC	Used to configure the GF9330 SDRAM controller. Set to ‘1’ when in 24-bit mode. This bit is auto-configured based on standard and mode selection.	Auto
	13	PROGRESSIVE_ INPUT	AC	When set to ‘1’, configures the GF9330 to accept a progressive video format. This bit is auto-configured based on standard and mode selection.	Auto
	15:14	ID_MODE[1:0]	AC	Defines the type of video sequence for input video de-multiplexing. When set to "00" the input represents a 4:2:2 sequence, "01" represents a 4:1:1 sequence, and "10" represents an HD format. This word can be auto-configured based on video standard and mode.	Auto
22	11:0	INPUT_H_BLANK_ WORDS_PER_LINE [11:0]	AC	Defines the number of horizontal blanked input words per line which corresponds to 2 times the number of blanking pixels per line for 4:2:2 SD modes and is equal to the number of pixels per line for HD formats. This value can be auto-configured.	Auto
	12	H_BLANK_SIZE_ 1HALF	AC	Reserved for output video formats requiring the equivalent of ½ pixel line size resolution. This occurs for STD 0, MODE 2 and 3 only.	Auto
	13	FIELD2_HAS_TOP_ LINE	AC	Set to ‘1’ when field 2 line one is the first line in the video frame (SMPTE 260M).	Auto
	14	EVEN_FIELD_ONE_ MORE	AC	Set to ‘1’ for video standards that have an even number of lines per frame (SMPTE 295M).	Auto
	15	ODD_FIELD_ONE_ MORE	AC	Set to ‘1’ for video standards that have an even number of lines per frame (SMPTE 295M).	Auto

Table 3-5: Control Register Definitions (Continued)

Address	Bit Location	Register Name	Class	Description	Default
23	9:0	NO_LINE_DELAYS [9:0]	AC	Defines the number of line delays to implement within the external field delay. This value is auto-configured based on standard and mode. The calculation is: No_line_delays = (Total number of lines per frame -7) / 2.	Auto
	11:10	FDC_MODE[1:0]	AC	Defines the field delay controller mode for output video formatting: 00: I to P mode 01: PsF to P 10: 30i to 24p 11: 30i to 24PsF	Auto
	12	FRAME_REGEN	AC	Defines frame timing regeneration. This occurs for all 30i-24p and 30i-24PsF modes.	Auto
	15:13	OM_MODE[2:0]	AC	Defines the GF9330 video output mode: 000: SD bypass 001: SD I to P or field merging 010: SD I to P 011: SD I to PsF 100: HD bypass 101: HD I to P or field merging 110: HD I to P 111: HD I to PsF This value can be auto-configured based on standard and mode.	Auto
24	12:0	OUTPUT_H_LINE_ SIZE[11:0]	AC	Represents the total number of pixels (Active plus blanking) per output line.	Auto
25	11:0	OUTPUT_H_BLANK _SIZE[11:0]	AC	Defines the number of blanking pixels per line at the output.	Auto
	15:12	F_VBI2_OFFSET[3:0]	AC	Defines the number of lines to wait before the rising F transition in the vertical blanking interval on the output.	Auto
26	11:0	V_BLANK1_LASTLINE [11:0]	UC	Defines the last line of the first blanking interval, where line 1 is the first blank line of the vertical blanking interval that precedes the odd field or first frame.	Auto
	15:12	F_VBI1_OFFSET[3:0]	AC	Defines the number of lines to wait before the falling F transition in the vertical blanking interval on the output.	Auto
27	11:10	V_FIELD1_LASTLINE [11:0]	UC	Defines the last line of the first active video field.	Auto
	14:12	ADD_LINES_BOTTOM _F2	UC	Defines the number of lines to add to the bottom of field 2 (not used).	Auto
28	11:10	V_BLANK2_LASTLINE [11:0]	UC	Defines the last line of the second blanking interval.	Auto
	14:12	ADD_LINES_BOTTOM _F1	UC	Defines the number of lines to add to the bottom of field 1 (not used).	Auto

Table 3-5: Control Register Definitions (Continued)

Address	Bit Location	Register Name	Class	Description	Default
29	11:0	V_FIELD2_LASTLINE [11:0]	UC	Defines the last line of the second active video field.	Auto
	14:12	ADD_LINES_TOP_F2	AC	Defines the number of lines to add to the top of field 2 (not used).	Auto
30	0	EXT_MEMCLK_SEL	AC	Controls the selection of the SDRAM clock source. For VCLK_IN frequency less than 36 MHz, the internal clock doubler can be used, in all other modes an external source is required (MEMCLK_IN).	Auto
	1	VOCLK_X1_SEL	AC	Normally set for HD modes where the output video clock is equal to the input video clock frequency and is set to '0' for SD cases where the output video clock is double the video input clock frequency.	Auto
	2	CLK_X1_SE	AC	Normally set for all HD modes and is '0' for all other cases.	Auto
31	0	START_OPERATION	UC	Using external F_IN, V_IN and H_IN signals, this parameter must be set following the completion of programming the F_IN, V_IN and H_IN offsets.	0
	15	CMD_RESET	UC	Forces the GF9330 to enter a reset state. This commanded reset remains in effect until this parameter is cleared with a subsequent command.	0

3.6 Closed Caption Blanking

The GF9330 provides a blanking function for selected input video lines. Consecutive lines within each input field are blanked when this function is enabled, beginning with the CC_BLANK_START_LINE and ending with the CC_BLANK_END_LINE. The blanking is applied prior to any processing of the video data.

The blanking function is enabled with the CC_BLANK_EN bit. BLANK_START_LINE and BLANK_END_LINE are each allocated 8-bits within the host interface.

3.7 Programmable Noise Reduction and Detail Enhancement

The GF9330 performs an efficient technique for high frequency noise reduction and detail enhancement. There are 256 levels of control provided by the NOISE_RED[7:0] bits within the host interface.

High frequency details that are detected with a two-dimensional high pass filter are enhanced using a non-linear function mapping between input and output signal. There are 512 levels of control provided by the DETAIL_ENH[9:0] bits within the host interface.

3.8 RESET

The $\overline{\text{RESET}}$ pin will reset all internal logic to it's default conditions when set LOW. On power up it is recommended to reset the device to ensure all internal registers are set to their default state. When applying a reset, the GF9330 will load in the STD[4:0] and MODE[2:0] settings from the external pins. If no further configuration is done, these settings will be used for the operation of the device.

3.9 Modes of Operation

The GF9330 supports stand-alone, co-processor enabled, pass-through and film rate down conversion modes of operation. Table 3-6: Modes of Operation: MODE[2:0] shows the basic operating modes for the GF9330 as selected using the MODE[2:0] control bits or through the host interface using the MODE[2:0] register, Address [0][7:5].

Table 3-6: Modes of Operation: MODE[2:0]

Mode	Description
000	Motion adaptive de-interlacing of input video signal.
001	De-interlacing of input video signal with pull-down compensation.
010	Film rate down conversion mode (60Hz -> 24Hz).
011	Film rate down conversion mode (60Hz -> 24Hz Segmented Frame)
100 to 110	Reserved
111	Video pass through mode.

3.9.1 De-Interlacing Mode (MODE=000)

When set to operate as a de-interlacer the GF9330 can operate as a “stand-alone” device performing motion adaptive processing. To enable multi-directional edge and vertical motion detection the GF9330 must be connected to the GF9331 as described in 3.3 Seamless Interface to the GF9331 Motion Co-processor for Directional Filter Control.

Segmented frame to progressive frame conversion is also supported in this mode. This function is performed when the progressive segmented frame input video format is selected on either the external pins or host interface register STD[4:0].

3.9.2 De-interlacing Mode with Pull-down Compensation (MODE=001)

When set to operate in this mode, the GF9330 can operate as a “stand-alone” device performing motion adaptive processing with added 3:2 pull-down compensation. To enable multi-directional edge and vertical motion detection the GF9330 must be connected to the GF9331 as described in 3.3 Seamless Interface to the GF9331 Motion Co-processor for Directional Filter Control.

The GF9330 will provide 3:2 sequence compensation (field merging) for film source material. When using internal 3:2 sequence detection, the GF9330 will perform "field-merging" for 3:2 sequences, or will revert to VT processing when no 3:2 sequence is identified. The 3:2 sequence can be internally detected (host interface bit, MODE_32 = 0), or supplied via the external sequence pins (XSEQ[3:0]) for MODE_32 = HIGH. With the external sequence selected, the device will revert back to VT processing if the external sequence pins have an invalid code (i.e. A to F). The XSEQ[3:0] value should be changed during the sixth blank line of each vertical blanking interval.

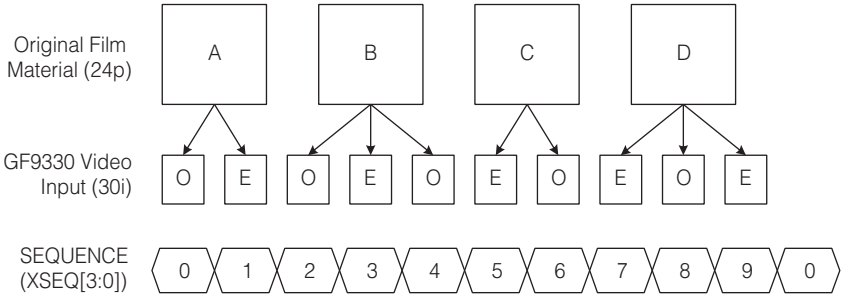


Figure 3-12: Sequence Detection Input Signals

3.9.3 Film Rate Down Conversion Mode (MODE= 010)

When configured to operate as a Film Rate Down Converter, the GF9330 removes 3:2 sequences from the input video stream and outputs 24Hz progressive scan video. No filtering of the signal is performed in this mode of operation. The external 3:2 sequence pins (XSEQ[3:0]) are used in this mode, the setting of the MODE_32 bit has no effect.

NOTE: In this mode, 3:2 compensation remains in effect at all times.

3.9.4 Film Rate Down Conversion Mode, Segmented Frame Output (MODE= 011)

This mode operates in the same manner as the Film Rate Down Converter mode, but outputs the progressive scan video in segmented frame format.

3.9.5 Video Pass Through Mode (MODE=111)

The GF9330, operating in Pass-through Mode, will pass through only the active portion of the input video signal. All other ancillary data will be lost from the input data stream.

The video channel is maintained in bypass mode, however, no processing takes place. Therefore, field buffers are still in use and the chip must be in a known programmed state.

3.10 Output Data Formats

The GF9330 supports multiple output data formats. The output data format depends on the input format selected as well as the defined operating mode.

Table 3-7: Output Formats specifies the available output formats for the GF9330.

Table 3-7: Output Formats

STD	Input Format	De-interlacing		Film Rate Down-Conversion		Bypass
		I-to-P Convert mode=000	Field Merging mode=001	I-to-P Convert mode=010	I-to-PsF Convert mode=011	mode=111
0	525i (30/1.001) SMPTE 125M	525p (60/1.001) SMPTE 293M See Note: [a]	525p (60/1.001) SMPTE 293M See Note: [a]	525p (24/1.001 See Note: [a]	525p (24/1.001) See Note: [a]	See Note: [a]
1	Reserved	NA	NA	NA	NA	
2	525i (30/1.001) SMPTE 267M - 16x9	525p (60/1.001) 16x9 See Note: [a]	525p (60/1.001) 16x9 See Note: [a]	525p (24/1.001) 16x9 See Note: [a]	525PsF (24/1.001) 16x9 See Note: [a]	See Note: [a]
3	Reserved					
4	625i (25) EBU Tech 3267	625p (50) ITU-R BT.1358 See Note: [a]	625p (50) ITU-R BT.1358 (2:2 Pulldown Comp.) See Note: [a]	625p (25) (2:2 Pulldown Comp.) See Note: [a]	625PsF (25) (2:2 Pulldown Comp.) See Note: [a]	See Note: [a]
5	Reserved					
6	625i (25) 16 x9 ITU-R BT.601 Part B	625p (50) 16 x 9 See Note: [a]	625p (50) 16 x 9 See Note: [a]	625p (25) 16 x 9 See Note: [a]	625PsF (25)16 x 9 See Note: [a]	See Note: [a]
7	Reserved					
8	525p (60/1.001) SMPTE 293M	NA	NA	NA	NA	See Note: [a]
9	Reserved					
10	Reserved					
11	Reserved					
12	625p (50) ITU-R BT-1358	NA	NA	NA	NA	See Note: [a]
13	625p (50) 16x9	NA	NA	NA	NA	See Note: [a]
14	Generic SD 4:1:1	Refer to 3.2.2 Generic Input Format Signalling				See Note: [a]
15	Generic SD 4:2:2	Refer to 3.2.2 Generic Input Format Signalling				See Note: [a]

Table 3-7: Output Formats (Continued)

STD	Input Format	De-interlacing		Film Rate Down-Conversion		Bypass
		I-to-P Convert mode=000	Field Merging mode=001	I-to-P Convert mode=010	I-to-PsF Convert mode=011	mode=111
16	720p (60 & 60/1.001) SMPTE 296M-2001	NA	NA	NA	NA	See Note: [b]
17	720p (30 & 30/1.001) SMPTE 296M-2001	NA	NA	NA	NA	See Note: [b]
18	1080p (30 & 30/1.001) SMPTE 274M	NA	NA	NA	NA	See Note: [b]
19	720p (50) SMPTE 296M-2001	NA	NA	NA	NA	See Note: [b]
20	1080p (25) SMPTE 274M	NA	NA	NA	NA	See Note: [b]
21	720p (25) SMPTE 296M-2001	NA	NA	NA	NA	See Note: [b]
22	1080p (24 & 24/1.001) SMPTE 274M	NA	NA	NA	NA	See Note: [b]
23	720p (24 & 24/1.001) SMPTE 296M-2001	NA	NA	NA	NA	See Note: [b]
24	1080i (30 & 30/1.001) SMPTE 274M	1080p (60 & 60/1.001) SMPTE 274M (System #1 and #2) See Note: [c]	1080p (60 & 60/1.001) SMPTE 274M (System #1 and #2) See Note: [c]	1080p (24 & 24/1.001) SMPTE 274M See Note: [b]	1080PsF (24 & 24/1.001) Draft RP May 99 See Note: [b]	See Note: [b]
25	1080PsF (30 & 30/1.001) SMPTE RP211-2000	1080p (30 & 30/1.001) SMPTE 274M See Note: [d]	NA	NA	NA	See Note: [b]

Table 3-7: Output Formats (Continued)

STD	Input Format	De-interlacing		Film Rate Down-Conversion		Bypass
		I-to-P Convert mode=000	Field Merging mode=001	I-to-P Convert mode=010	I-to-PsF Convert mode=011	mode=111
26	1080i (25) SMPTE 274M	1080p (50) SMPTE 274M (System #3) See Note: c	1080p (50) SMPTE 274M (System #3) (2:2 Pulldown Comp.) See Note: c	1080p (25) SMPTE 274M (System #9) (2:2 Pulldown Comp.) See Note: b	NA	See Note: b
27	1080PsF (25) SMPTE RP211-2000	1080p (25) SMPTE 274M (System #9) (PsF to P) See Note: d	NA	NA	NA	See Note: b
28	1080i (25) SMPTE 295M	1080p (50) SMPTE 295M (System #1) See Note: c	1080p (50) SMPTE 295M (System #1) (2:2 Pulldown Comp.) See Note: c	1080p (25) SMPTE 274M (System #9) (2:2 Pulldown Comp.) See Note: b	NA	See Note: b
29	1080PsF (24 & 24/1.001) SMPTE RP211-2000	1080p (24 & 24/1.001) SMPTE 274M (System #10 & #11) (PsF to P) See Note: d	NA	NA	NA	See Note: b
30	1035i (30 & 30/1.001) SMPTE 260M	1035p (60&60/1.001) See Note: c	1035p (60&60/1.001) See Note: c	1035p (24&24/1.001) See Note: b	1035p (24&24/1.001) See Note: b	See Note: b
31	Generic HD 4:2:2	Refer to 3.2.2 Generic Input Format Signalling				See Note: b

a.Y/C output multiplexed on Y1_OUT[11:0].
b. Y Output on Y1_OUT[11:0] C Output on C1_OUT[11:0].
c.Odd (first) pixel Y data on Y1_OUT[11:0], Even (second) pixel Y data on Y2_OUT[11:0], Odd (first) pixel C data on C1_OUT[11:0], Even (second) pixel C data on C2_OUT[11:0].
d.These standards cannot be used in stand alone mode. OM_MODE[2:0] register within the host interface must be configured to “110” in order to achieve output port operation as described in b.

3.10.1 Output Video Frame Cropping

The GF9330 provides programmable output video cropping in both the horizontal and vertical directions. Any rectangular window within the full output active frame (or field) is selectable for output, with all video data outside of this rectangular window cropped (set to the blanking level). The H_OUT, V_OUT, F_OUT signals are generated to provide timing for the cropped video frame. The embedded TRSs remain in the original positions.

Output video cropping is enabled with the CROP_EN bit within the host interface.

Cropping in the horizontal direction is implemented based on the settings of the CROP_H_CROP_SIZE and CROP_H_LINE_SIZE. The CROP_H_CROP_SIZE parameter specifies the number of active pixels to blank at the beginning of each line. The CROP_H_LINE_SIZE parameter specifies the length of the line to output, following the cropped pixels on the left side of the line. CROP_H_CROP_SIZE and CROP_H_LINE_SIZE are each allocated 12-bits within the host interface.

Cropping in the vertical direction is implemented based on the settings of the CROP_V_CROP_SIZE and CROP_V_FRAME_SIZE. The CROP_V_CROP_SIZE parameter specifies the number of active lines to blank at the beginning of each frame. The CROP_V_FRAME_SIZE parameter specifies the number of lines to output, following the cropped lines at the top of the frame (or field). CROP_V_CROP_SIZE and CROP_V_FRAME_SIZE are each allocated 12-bits within the host interface.

Valid H_OUT, V_OUT and F_OUT are always present even when output signals contain embedded TRS signals. When outputting one of the standards with embedded TRSs, H_OUT, V_OUT and F_OUT is synchronized with the GF9330's output data stream (V_OUT and F_OUT transition on EAV sequences).

Refer to Figure 3-13: Output Video Cropping for a pictorial representation of the cropping function.

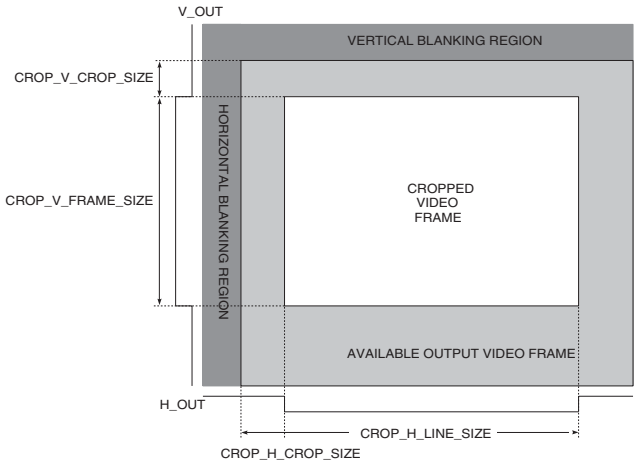


Figure 3-13: Output Video Cropping

3.10.2 12-bits Output Resolution

All output data busses are 12-bits in total resolution. Output Y data is always an unsigned data format. Output Cr Cb is always in a offset binary data format. Relative to the input data stream the 12-bits outputs are formatted as 10.2 (2 LSB extensions).

3.10.3 Controllable Rounding and Clipping on Output Data

The GF9330 provides a wide range of round/clipping options based on the setting of CL_RND[2:0] bits within the host interface as shown in Table 3-8: CL_RND[2:0].

Table 3-8: CL_RND[2:0]

CL_RND[2]	CL_RND[1]	CL_RND[0]	Description
0	0	0	12-bit Output. All channels rounded to 10.2 output resolution.
0	0	1	10-bit Output #1. Data clipped/rounded to 0 to 1023.
0	1	0	10-bit Output #2. Data clipped/rounded to 4 to 1019.
0	1	1	10-bit Output #3. Y data clipped/rounded 64 to 940. Cr/Cb clipped/rounded 64 to 960.
1	0	0	Reserved
1	0	1	8-bit Output #1. Data clipped/rounded to 0 to 255.
1	1	0	8-bit Output #2. Data clipped/rounded to 1 to 254.
1	1	1	8-bit Output #3. Y data clipped/rounded 16 to 235. Cr/Cb clipped/rounded 16 to 240.

3.11 Sequence Detection

The GF9330 supports two modes of operating with respect to 3:2 sequence detection (internal and external modes) as described in Table 3-9: 3:2 Mode Select. One bit in the host interface is reserved for the MODE_32 bit.

Table 3-9: 3:2 Mode Select

MODE_32	Description
0	Internal. The 3:2 sequence is automatically detected in the input data stream. The GF9330 reports 3:2 lock and 3:2 sequence information in the host interface registers called LOCK_32 and SEQUENCE[3:0]. The GF9330 also reports this information on the XSEQ[3:0] pins when configured as outputs.
1	External. The GF9330 accepts a 3:2 sequence from the XSEQ[3:0] pins configured as inputs.

3.11.1 Internal 3:2 Detection

When set to operate in internal 3:2 detect mode, the GF9330 can automatically detect a 3:2 pull-down sequence in the incoming video data stream. If a 3:2 sequence is detected, the GF9330 sets the LOCK_32 control bit in the host interface to '1'. The LOCK_32 pin is also asserted HIGH once the sequence has been detected.

The actual 3:2 sequence information is reported in the SEQUENCE[3:0] register within the host interface and on the XSEQ[3:0] pins. Refer to Figure 3-12: Sequence Detection Input Signals for a pictorial representation of the 3:2 sequence reporting.

3.11.2 External 3:2 Detection

When set to operate in external mode, the user will supply the 3:2 sequence information to the XSEQ[3:0] pins. The GF9330 uses this information to properly de-interlace the input signal or to perform 60Hz to 24Hz conversion depending on the state of the MODE[2:0] register in the host interface or MODE[2:0] pins.

When operating in this mode the input 3:2 sequence information relates to the input data stream. The 3:2 sequence information requires updating during the first blank line of the vertical blanking interval, identifying the sequence number for the following field.

3.11.3 Sequence Detection and Compensation

The GF9330 supports external 2:2 sequence detection. A LOCK_22 pin is provided to indicate the presence of a 2:2 sequence. The sequence information is inherently embedded in the interlaced video input data, and is identified with the F_IN signal (either derived from the embedded TRSs or supplied from the external pin). The LOCK_22 signal will be updated during the first line of each vertical blanking interval.

3.11.4 Static and Freeze Frame Detection/Compensation

The GF9330 operates in either disabled, automatic or manual mode for detection and compensation of freeze frame conditions within the video input stream. When set to operate in disabled mode (host interface bits, FF_MODE=10), the GF9330 disables the internal freeze frame detection and compensation circuitry and also ignores any information presented to the FF_EN pin or the host interface bit, FF_EN_BIT. When set to operate in automatic mode (FF_MODE[2:0]=01) the GF9330 internally detects and compensates for freeze frame situations. When a freeze frame situation is detected, the GF9330 reports this in the FF_DETECT status bit found in the host interface. This bit is updated at the beginning of a field and remains valid for the remainder of the field. When set to operate in manual mode (FF_MODE=00) the GF9330 monitors the FF_EN pin and the host interface bit, FF_EN_BIT to enable or disable freeze frame compensation. Static and freeze frame detection compensation is further described in Table 3-10: FF_MODE[1:0].

In order to manually force the freeze frame detector in the GF9330 into freeze in static or freeze in motion, the following parameters must be set as follows:

1. Freeze in Static: Uses the temporal filter only.

   MSF = 7FFFh
   FF_DET_HV = 0000h
   FF_EN_BIT = 1
2. Freeze in motion: Uses both the vertical and temporal filter.

   MSF = 0000h
   FF_DET_HV = FFFFh
   FF_EN_BIT = 0

NOTE: When using the freeze in motion settings when the image is static, there will be vertical ringing along the horizontal edges.

Table 3-10: FF_MODE[1:0]

Host Interface FF_MODE[1:0] Register	External FF_EN Pin	Host Interface FF_EN_BIT	Description
00	0	0	Manual: freeze frame detection and compensation disabled
	0	1	Manual: perform freeze frame compensation
	1	0	
	1	1	
01	x	x	Automatic freeze frame detection/compensation
10	x	x	Freeze frame detection and compensation disabled
11	x	x	Reserved

3.11.5 Motion Detection and Compensation

The GF9330 operates in disabled or automatic mode for motion detection and compensation. When set to operate in disable mode (host interface bits,

MD_MODE=00), the GF9330 does not perform internal motion detection and compensation. When set to operate automatic mode (MD_MODE=01) the GF9330 internally detects and compensates for motion. Motion detection and compensation control is further described in Table 3-11: MD_MODE[1:0].

Table 3-11: MD_MODE[1:0]

Host Interface MD_MODE[1:0] Register	Description
00	Disabled Mode
01	Automatic Mode
10	Reserved
11	Reserved

3.11.6 Processing Latency

In de-interlacing mode (with the exception of progressive segmented frame to progressive format conversion), the GF9330 processing latency is constant regardless of input or output format selection. In all other modes, (including progressive segmented frame to progressive format conversion and Film Rate Down Conversion) the GF9330 processing latency is unique yet constant regardless of input or output format selection.

For standard de-interlacing the delay will be 1 field 6 lines and 91 pixels.

For 3:2 detection and compensation to both 24p and 24psf the delay will be 1 frame 4 lines and 8 pixels.

In bypass mode the delay is always 569 lines.

4. Package Dimensions

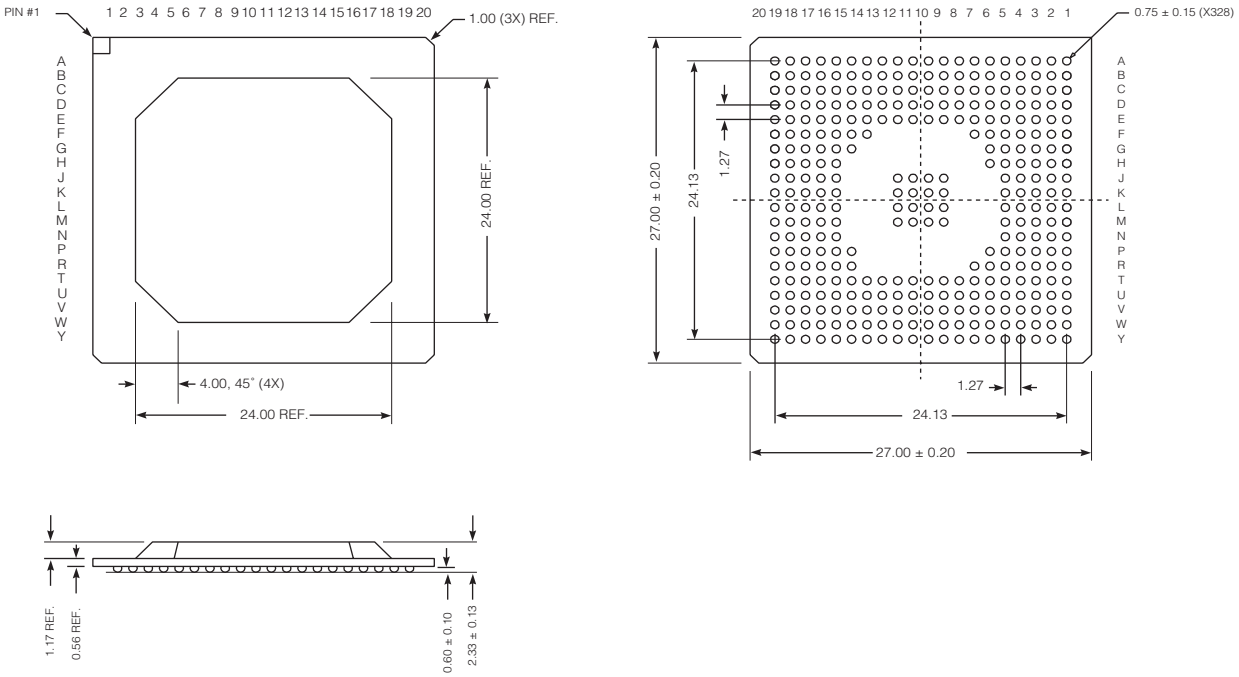


Figure 4-1: Package Dimensions

Revision History

Version	ECR	Date	Changes and / or Modifications
4	133231	June 2004	Correction to text for bypass mode and memories used. Changed document template.
3		October 2002	Update to document information and figures.

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DOCUMENT IDENTIFICATION

DATA SHEET

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